CLAIMS

1. A method for shaping a baseband signal comprising:

providing a plurality of coefficient memories, each having a plurality of coefficients values representing filter response waveform values;

determining a coefficient memory address for each of the coefficient memories;

addressing each of the plurality of coefficient memories;

retrieving an addressed coefficient value from each of the plurality of coefficient memories;

providing a negative value for each of the retrieved ones of the plurality of coefficient values;

selecting in response to the baseband signal, one of the retrieved coefficient value and the negative value; and

summing the selected value from each coefficient memory for providing a shaped signal.

2. The method of Claim 1 further comprising sharing the plurality of coefficient memories for shaping both an in-phase baseband signal and a quadrature baseband signal.

3. The method of Claim 2 wherein sharing the plurality of memories comprises:

retrieving one of the coefficient values corresponding to the in-phase baseband signal on a first edge of a clock signal; and

retrieving one of the coefficient values corresponding to the the quadrature baseband signal on a different second edge of the clock signal.

4. The method of Claim 3 wherein the clock signal comprises a digital to analog converter clock signal.

5. The method of Claim 1 wherein determining a coefficient memory address

comprises:

determining an increment for providing a predetermined number of samples for each of a plurality of symbols comprising the baseband signal; and

incrementing an address counter in response to the predetermined number of samples for each symbol and a predetermined coefficient memory size.

6. The method of Claim 1 wherein the baseband signal comprises an in-phase signal and a quadrature signal;

wherein selecting the coefficient value comprises selecting an in-phase value in response to the in-phase signal and selecting a quadrature value in response to the quadrature signal; and

wherein summing the selected value comprises summing the selected in phase value from each coefficient memory for providing a shaped in phase signal and summing the selected quadrature value from each coefficient memory for providing a shaped quadrature signal.

7. The method of Claim 1 wherein the negative value comprises at least one of:

a 2's complement value;

an offset binary value; and

a signed magnitude value.

8. The method of Claim 1 wherein providing a plurality of coefficient memories comprises combining at least two filter coefficients for forming the plurality of coefficient values such that coefficient memory storage is minimized.

9. The method of Claim 1 further wherein providing a plurality of coefficient memories further comprises providing coefficient memories corresponding to a plurality of roll-off factors.

10. The method of Claim 1 wherein the plurality of coefficient memories further includes one of:

the sum of a first filter response value and a second filter response value; and

the difference of a first filter response value and a second filter response value.

11. The method of Claim 10 wherein the first filter response and the second filter response are symmetric.

12. The method of Claim 10 wherein retrieving coefficient values comprises:
providing an address counter having a plurality of logic outputs for addressing the coefficient memories; and
determining whether to retrieve one of the sum and the difference in response to selected ones of the logic outputs.

13. The method of Claim 12 further comprising:
providing a logic circuit having an output, a first input coupled to a logic output of the address counter, a second input coupled to an in-phase data symbol bit and a third input coupled to a quadrature data symbol bit;
determining whether to select one of the retrieved value and the negative value in response to the output of the logic circuit.

14. The method of Claim 10 wherein summing the selected value comprises:
providing a plurality of adder stages, each adder coupled to a pipeline register;
clocking the pipeline register at a digital to analog converter (D/A) rate; and
scaling and formatting the summed values after a final adder stage.

15. The method of Claim 10 wherein the baseband signal is clocked at a symbol rate and the retrieval of coefficients is clocked at a digital to analog converter (D/A) rate such that the number of retrievals per coefficient equals the D/A rate divided by the symbol rate.

16. The method of Claim 10 wherein the filter waveform comprises a raised cosine.

17. The method of Claim 10 wherein the filter waveform comprises a square root raised cosine.

18. A method for shaping a baseband signal comprising:
providing a plurality of digital words, each digital word indicating a

coefficient value at an instant of time;

selecting responsive to the baseband signal, one of the digital words and a corresponding negative value of the digital word; and

summing the selected digital word for providing a baseband shaped signal.

19. The method of Claim 18 wherein providing a plurality of digital words comprises combining at least two filter coefficients for forming the plurality of coefficient values such that coefficient memory storage is minimized.

20. A device comprising:

a plurality of coefficient memories, each memory having an input address bus, a multiplexor input and a coefficient value output;

a plurality of first registers, each having an input coupled to a respective one of the coefficient value outputs, a digital to analog (D/A) clock input and an output;

a plurality of negative value circuits, each circuit having an input coupled to a respective one of the first register outputs, and an output;

a plurality of 2:1 multiplexors, each having a first input coupled to a respective one of the first register outputs and having a second input coupled to a respective one of the output of the plurality of negative value circuits ;

a plurality of second registers, each having an input coupled to a respective one of the outputs of the plurality of 2:1 multiplexors, a digital to analog (D/A) clock input and an output; and

an adder having a plurality of inputs coupled to respective ones of the plurality of second registers.

21. The device of Claim 20 wherein each of the plurality of negative value circuits comprises at least one of:

a 2's complement logic element;

an offset binary logic element; and

a signed magnitude logic element.

22. The device of Claim 20 further comprising a coefficient address generator having an output coupled to a coefficient memory input address bus, the input address having a plurality of address lines.

23. The device of Claim 22 wherein the coefficient address generator further comprises:

an adder having a plurality of address output lines;

an address register coupled to the plurality of address output lines and having clocked address line outputs and an address counter most significant bit output;

an exclusive or logic gate (XOR) array having address inputs coupled to the clocked address lines outputs and an address counter most significant bit input coupled to the address counter most significant bit output, and outputs coupled to a corresponding plurality of the plurality of address lines of the coefficient memory address bus; and

an XOR multiplexor having inputs coupled a pair of baseband bit signals and an output coupled to one of the plurality of address lines of the coefficient memory address bus.